

Amdt. dated April 13, 2005
Reply to Office action of Jan. 13, 2005

Serial No. 10/077,104
Docket No. SJO920010085US1
Firm No. 0037.0019

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method for processing operations in a system including a bus, a target device and devices capable of accessing the target device over the bus, wherein the target device performs:

receiving a transaction write request from one of the devices over the bus;

determining whether a delayed read request is pending after receiving the transaction write request;

issuing a command to disconnect the device initiating the transaction write request from the bus in response to determining that the delayed read request is pending; and

allowing the device initiating the transaction write request to reconnect to the bus and complete the transaction write request after the delayed read request is completed.

2. (Currently Amended) The method of claim 1, wherein the delayed read request is directed toward a first memory region and the transaction write request ~~comprises an~~ Input/Output request is directed toward a second memory region.

3. (Previously Presented) The method of claim 2, wherein the first and second memory regions are implemented within the target device.

4. (Original) The method of claim 1, wherein the command to disconnect comprises a retry disconnect that occurs before data subject to the transaction write request is transmitted.

5. (Currently Amended) The method of claim 1, further comprising:
determining whether requested data for the delayed read request is available to return, wherein the command to disconnect the device initiating the transaction write request is issued after the requested data for the delayed read request is determined to be available to return.

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6. (Currently Amended) ~~The method of claim 5, further comprising:~~ A method for processing operations in a system including a bus, a target device and devices capable of accessing the target device over the bus, wherein the target device performs:
receiving a transaction request from one of the devices over the bus;
determining whether a delayed read request is pending after receiving the transaction request;
determining whether requested data for the delayed read request is available to return;
issuing a command to disconnect the device initiating the transaction request from the bus in response to determining that the delayed read request is pending and the requested data for the delayed read request is determined to be available to return;
allowing the device initiating the transaction request that was disconnected in response to the command to reconnect to the bus and complete the transaction request after the delayed read request is completed; and
allowing the transaction request to proceed if the delayed read request is pending and if the requested data for the delayed read request is not available to return.

7. (Original) The method of claim 6, further comprising:
after allowing the transaction request to proceed, determining that all the requested data is available to return, wherein the command to disconnect is issued after determining that all the requested data is available to return after allowing the transaction request to proceed.

8. (Original) The method of claim 7, wherein the transaction request will attempt to reconnect to the target device to complete an unfinished portion of the transaction request that did not complete as a result of the issuing of the command to disconnect.

9. (Original) The method of claim 8, wherein the transaction request comprises a write request, wherein the target device receives write data while the delayed read request is pending and the requested data is not available to return, wherein the device issuing the write request will transmit that portion of the write data not sent as a result of the issuing of the command to disconnect during a subsequent reconnect to the target device.

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10. (Currently Amended) The method of claim 1, wherein the bus, target device, and devices communicate using the Peripheral Component Interconnect (PCI) protocol, and wherein the devices that initiate the delayed read request and transaction write request comprise master devices for the bus.

11. (Currently Amended) The method of claim 1, further comprising:
determining whether a variable indicates a first state or a second state, wherein the state indicated by the variable determines when the target device issues the command to disconnect the device initiating the transaction write request while the delayed read request is pending.

12. (Currently Amended) The method of claim 11, further comprising:
issuing the command to disconnect the device initiating the transaction write request when the device that initiated the delayed read request attempts to reconnect to the target device if the variable indicates the first state; and
issuing the command to disconnect the device initiating the transaction write request after all the requested data for the delayed read request is determined to be available to return if the variable indicates the second state.

13. (Currently Amended) The method of claim 12, further comprising:
allowing the transaction write request to proceed during a time at which all the requested data for the delayed read request is not available to return if the variable indicates the second state.

14. (Currently Amended) The method of claim 1, wherein transaction write request and delayed read request are initiated from different devices.

15. (Currently Amended) A system for processing operations in communication with devices, comprising:
a target device;
a bus, wherein the devices are capable of accessing the target device over the bus;
means for receiving a transaction write request from one of the devices over the bus;

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means for determining whether a delayed read request is pending after receiving the transaction write request;

means for issuing a command to disconnect the device initiating the transaction write request from the bus in response to determining that the delayed read request is pending;
and

means for allowing the device initiating the transaction write request to reconnect to the bus and complete the transaction write request after the delayed read request is completed.

16. (Currently Amended) The system of claim 15, further comprising:
a first memory region; and
a second memory region, wherein the delayed read request is directed toward the first memory region and the transaction write request comprises an Input/Output request is directed toward the second memory region.

17. (Currently Amended) The system of claim 15, further comprising:
means for determining whether requested data for the delayed read request is available to return, wherein the command to disconnect the device initiating the transaction write request is issued after the requested data for the delayed read request is determined to be available to return.

18. (Currently Amended) ~~The system of claim 17, further comprising:~~ A system for processing operations in communication with devices, comprising:

a target device;
a bus, wherein the devices are capable of accessing the target device over the bus;
means for receiving a transaction request from one of the devices over the bus;
means for determining whether a delayed read request is pending after receiving the transaction request;
means for issuing a command to disconnect the device initiating the transaction request from the bus in response to determining that the delayed read request is pending and the requested data for the delayed read request is determined to be available to return;

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means for allowing the transaction request to proceed if the delayed read request is pending and if the requested data for the delayed read request is not available to return;

means for allowing the device initiating the transaction request that was disconnected in response to the command to reconnect to the bus and complete the transaction request after the delayed read request is completed; and

means for allowing the transaction request to proceed if the delayed read request is pending and if the requested data for the delayed read request is not available to return.

19. (Original) The system of claim 18, further comprising:

means for determining that all the requested data is available to return after allowing the transaction request to proceed, wherein the command to disconnect is issued after determining that all the requested data is available to return after allowing the transaction request to proceed.

20. (Original) The system of claim 19, wherein the transaction request will attempt to reconnect to the target device to complete an unfinished portion of the transaction request that did not complete as a result of the issuing of the command to disconnect.

21. (Original) The system of claim 15, wherein the bus, target device, and devices communicate using the Peripheral Component Interconnect (PCI) protocol.

22. (Currently Amended) The system of claim 15, further comprising:

means for determining whether a variable indicates a first state or a second state, wherein the state indicated by the variable determines when the target device issues the command to disconnect the device initiating the transaction write request while the delayed read request is pending.

23. (Currently Amended) An article of manufacture including code for processing operations in a system including a bus, a target device and devices capable of accessing the target device over the bus, wherein the code causes the target device to perform:

receiving a transaction write request from one of the devices over the bus;

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determining whether a delayed read request is pending after receiving the transaction write request;

issuing a command to disconnect the device initiating the transaction write request from the bus in response to determining that the delayed read request is pending; and

allowing the device initiating the transaction write request to reconnect to the bus and complete the transaction write request after the delayed read request is completed.

24. (Currently Amended) The article of manufacture of claim 23, wherein the delayed read request is directed toward a first memory region and the transaction write request comprises an Input/Output request is directed toward a second memory region.

25. (Previously Presented) The article of manufacture of claim 24, wherein the first and second memory regions are implemented within the target device.

26. (Currently Amended) The article of manufacture of claim 23, wherein the command to disconnect comprises a retry disconnect that occurs before data subject to the transaction write request is transmitted.

27. (Currently Amended) The article of manufacture of claim 23, further comprising: determining whether requested data for the delayed read request is available to return, wherein the command to disconnect the device initiating the transaction write request is issued after the requested data for the delayed read request is determined to be available to return.

28. (Currently Amended) ~~The article of manufacture of claim 27, further comprising:~~
An article of manufacture including code for processing operations in a system including a bus, a target device and devices capable of accessing the target device over the bus, wherein the code causes the target device to perform:

receiving a transaction request from one of the devices over the bus;

determining whether a delayed read request is pending after receiving the transaction request;

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determining whether requested data for the delayed read request is available to return;
issuing a command to disconnect the device initiating the transaction request from the bus
in response to determining that the delayed read request is pending and the requested data for the
delayed read request is determined to be available to return;
allowing the device initiating the transaction request that was disconnected in response to
the command to reconnect to the bus and complete the transaction request after the delayed read
request is completed; and
allowing the transaction request to proceed if the delayed read request is pending and if
the requested data for the delayed read request is not available to return.

29. (Original) The article of manufacture of claim 28, further comprising:
after allowing the transaction request to proceed, determining that all the requested data is
available to return, wherein the command to disconnect is issued after determining that all the
requested data is available to return after allowing the transaction request to proceed.

30. (Original) The article of manufacture of claim 29, wherein the transaction request
will attempt to reconnect to the target device to complete an unfinished portion of the transaction
request that did not complete as a result of the issuing of the command to disconnect.

31. (Original) The article of manufacture of claim 30, wherein the transaction request
comprises a write request, wherein the target device receives write data while the delayed read
request is pending and the requested data is not available to return, wherein the device issuing the
write request will transmit that portion of the write data not sent as a result of the issuing of the
command to disconnect during a subsequent reconnect to the target device.

32. (Currently Amended) The article of manufacture of claim 23, wherein the bus,
target device, and devices communicate using the Peripheral Component Interconnect (PCI)
protocol, and wherein the devices that initiate the delayed read request and transaction write
request comprise master devices for the bus.

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33. (Currently Amended) The article of manufacture of claim 23, further comprising:
determining whether a variable indicates a first state or a second state, wherein the state indicated by the variable determines when the target device issues the command to disconnect the device initiating the transaction write request while the delayed read request is pending.

34. (Currently Amended) The article of manufacture of claim 33, further comprising:
issuing the command to disconnect the device initiating the transaction write request when the device that initiated the delayed read request attempts to reconnect to the target device if the variable indicates the first state; and
issuing the command to disconnect the device initiating the transaction write request after all the requested data for the delayed read request is determined to be available to return if the variable indicates the second state.

35. (Currently Amended) The article of manufacture of claim 34, further comprising:
allowing the transaction write request to proceed during a time at which all the requested data for the delayed read request is not available to return if the variable indicates the second state.

36. (Currently Amended) The article of manufacture of claim 23, wherein the transaction write request and the delayed read request are initiated from different devices.